

**CN432 GNSS Receiver Design II: Baseband Signal Processing and Implementation**  
**September 20, 2010, 1:30 pm-5:00 pm, CEU: 3.0**  
**GNSS Solutions® Tutorials prior to ION GNSS 2010, September 20-21, 2010**  
**Oregon Convention Center, Portland, Oregon, USA**

**Instructor:** Dr. Sanjeev Gunawardena, Ohio University

**Prerequisite:** Some knowledge of mathematics, digital circuits, computer science, digital signal processing and GNSS will be useful. Part I of this two-part sequence, CN431: GNSS Receiver Design I: RF Front End Theory and Design is highly recommended as a pre-requisite for this course.

**Intended Audience:** Design and development engineers, academic researchers, scientists, educators, and managers interested in the area of satellite navigation, particularly with respect to the design and implementation of GNSS receivers, software radio research platforms, or GNSS signal processors.

**Notes Provided:** Slides presented will be professionally spiral bound, with clear plastic cover, including color to add clarity where needed.

**Reference List:** A reference list will be provided as part of the note package for completeness and to allow the interested attendee to obtain additional information.

**Course Overview:** This course is the second of a two-part sequence covering the design and practical implementation of GNSS receivers using the latest developments in radio frequency (RF) and digital signal processing technologies. The material covered will be applicable to a wide range of GNSS user equipment from instrumentation-quality reference receivers through aviation-grade, military, and low-power consumer-grade single chip devices. Part 1 covers the design of single and multiband GNSS RF front-ends starting from the low-noise amplifier (LNA) through to the analog-to-digital converter (ADC). Part 2 covers digital signal processing techniques from sample correlation through range measurement computation, and the implementation of these techniques using hardware, software, or reconfigurable logic (i.e. FPGA) processors. The course material is approached with both the theoretical and practical perspective, using case studies of actual GNSS receivers developed by the instructor as well as an overview of the latest commercially available GPS chipsets.

**Course Content:**

- Overview of received GNSS signals: Signal structures of GPS L1-C/A, L2C, and L5 and Galileo E1. BPSK, BOC, TMBOC, and other proposed modernized signal modulations and properties.
- Signal correlation: Time, frequency, and transform-domain techniques. The complementary nature of time-domain and frequency-domain processing. Coherent versus non-coherent integration. Advanced correlator architectures for multipath mitigation and signal quality/deformation monitoring (SQM, SDM).

- Processing complexity: Methods for reducing complexity for realtime implementation. Performance impact due to reduced numerical precision.
- Signal Acquisition: Acquisition threshold statistics, search algorithms, fast acquisition techniques
- Acquisition-to-tracking transition: Acquisition verification, bit synchronization, and false-lock detection techniques.
- Tracking: FLL, PLL and DLL, loop tightening/transitioning techniques, noise bandwidth, tracking performance, block (batch) processing and loopless tracking techniques.
- Measurement computation: Navigation databit extraction and decoding, TOT and TOR counters, pseudorange and carrier-phase measurements, carrier-smoothed code.
- Implementation techniques and platforms (including case studies):
  - Matlab®-based non-realtime algorithms
  - Bitwise software algorithms for general-purpose microprocessors
  - FPGA-based processing engines and design overview
  - Commercial GPS processor chipsets

**Course Outcomes:** At the completion of this course, the attendee should have a solid understanding of the fundamentals of GNSS receiver baseband signal processing including the many options and sources available for implementing your own GNSS receiver prototype or research testbed.